Designation: F 1392 – 00

Standard Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements With a Mercury Probe[1]

1. Scope

1.1 This test method[2] covers the measurement of net carrier density and net carrier density profiles in epitaxial and polished bulk silicon wafers in the range from about 4×10^{13} to about 8×10^{16} carriers/cm^3 (resistivity range from about 0.1 to about 100 Ω·cm in *n*-type wafers and from about 0.24 to about 330 Ω·cm in *p*-type wafers).

1.2 This test method requires the formation of a Schottky barrier diode with a mercury probe contact to an epitaxial or polished wafer surface. Chemical treatment of the silicon surface may be required to produce a reliable Schottky barrier diode **(1)**.[3] The surface treatment chemistries are different for *n*- and *p*-type wafers. This test method is sometimes considered destructive due to the possibility of contamination from the Schottky contact formed on the wafer surface; however, repetitive measurements may be made on the same test specimen.

1.3 This test method may be applied to epitaxial layers on the same or opposite conductivity type substrate. This test method includes descriptions of fixtures for measuring substrates with or without an insulating backseal layer.

1.4 The depth of the region that can be profiled depends on the doping level in the test specimen. Based on data reported by Severin **(1)** and Grove **(2)**, Fig. 1 shows the relationships between depletion depth, dopant density, and applied voltage together with the breakdown voltage of a mercury silicon contact. The test specimen can be profiled from approximately the depletion depth corresponding to an applied voltage of 1 V to the depletion depth corresponding to the maximum applied voltage (200 V or about 80 % of the breakdown voltage, whichever is lower). To be measured by this test method, a layer must be thicker than the depletion depth corresponding to an applied voltage of 2 V.

1.5 This test method is intended for rapid carrier density determination when extended sample preparation time or high temperature processing of the wafer is not practical.

NOTE 1—Test Method F 419 is an alternative method for determining net carrier density profiles in silicon wafers from capacitance-voltage measurements. This test method requires the use of one of the following structures: (*1*) a gated or ungated *p-n* junction diode fabricated using either planar or mesa technology or (*2*) an evaporated metal Schottky diode.

1.6 This test method provides for determining the effective area of the mercury probe contact using polished bulk reference wafers that have been measured for resistivity at 23°C in accordance with Test Method F 84 (Note 2). This test method also includes procedures for calibration of the apparatus for measuring both capacitance and voltage.

NOTE 2—An alternative method of determining the effective area of the mercury probe contact that involves the use of reference wafers whose net carrier density has been measured using fabricated mesa or planar *p-n* junction diodes or evaporated Schottky diodes is not included in this test method but may be used if agreed upon by the parties to the test.

1.7 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.* Specific hazard statements are given in 7.1, (7.2, 7.10.3 (Note 7), 8.2, 11.5.1, 11.6.3, and 11.6.5.

2. Referenced Documents

2.1 *ASTM Standards:*

D 5127 Guide for Ultra Pure Water Used in the Electronics and Semiconductor Industry[4]

D 4356 Practice for Establishing Consistent Test Method Tolerances[5]

E 691 Practice for Conducting an Interlaboratory Study to

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[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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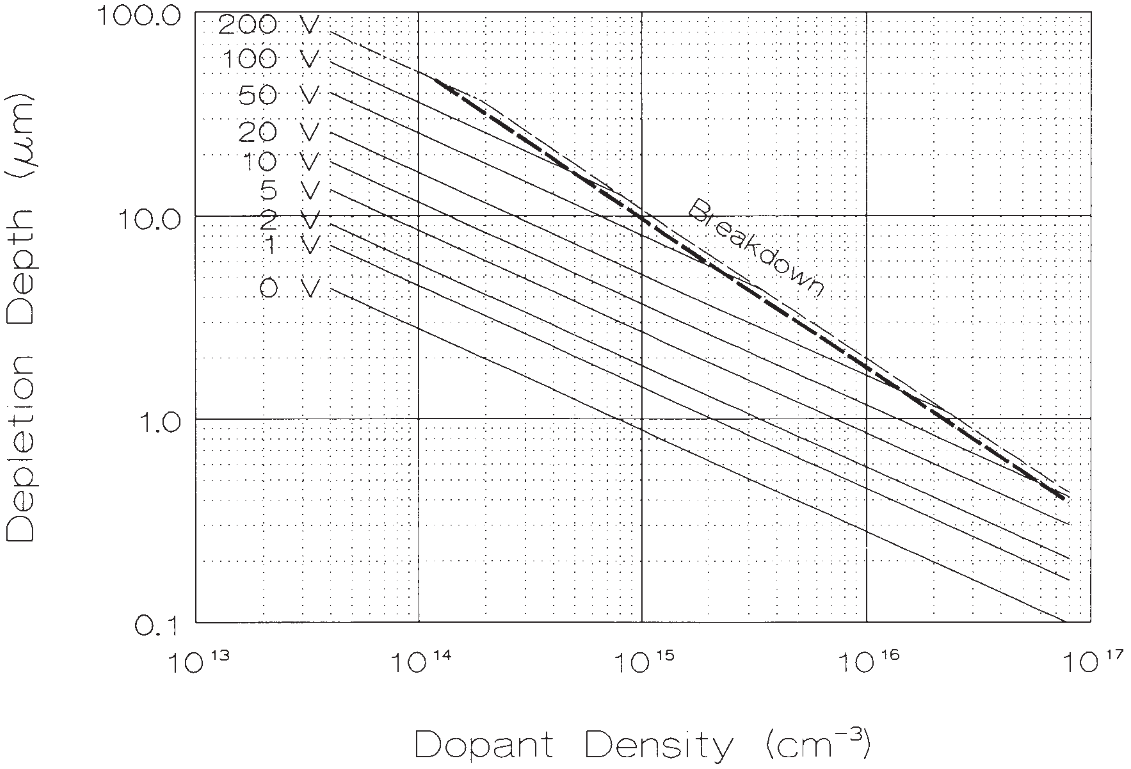
[2] DIN 50439, Determination of the Dopant Concentration Profile of a Single Crystal Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact, is technically equivalent to this test method. DIN 50439 is the responsibility of DIN Committee NMP 221, with which Committee F-1 maintains close liaison. DIN 50439 is available from Beuth Verlag GmbH, Burggrafenstraße 4-10, D-1000, Berlin 30, Germany.

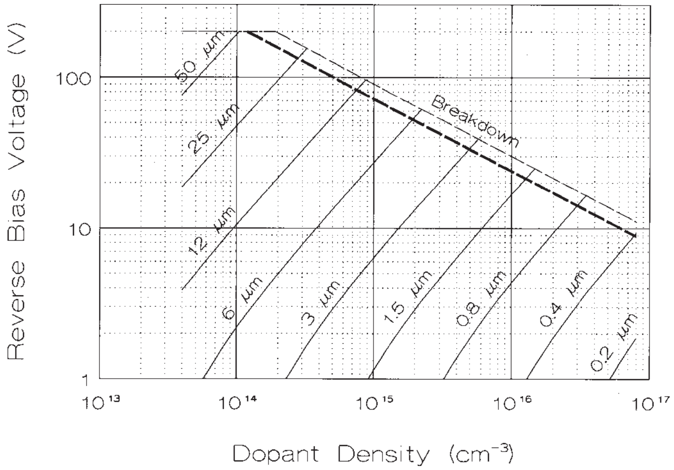
[3] The boldface numbers in parentheses refer to the list of references at the end of this test method.

[4] *Annual Book of ASTM Standards*, Vol 11.01.

[5] *Annual Book of ASTM Standards*, Vol 14.02.



(a) Depletion Depth as a Function of Dopant Density with Applied Reverse Bias Voltage as a Parameter.



(b) Applied Reverse Bias Voltage as a Function of Dopant Density with Depletion as a Parameter.

NOTE 1—The light dashed line represents the applied reverse bias voltage at which breakdown occurs in a mercury-silicon contact; the heavy dashed line represents 80 % of this voltage, it is recommended that the applied reverse bias voltage not exceed this value. The light chain-dot line represents the maximum reverse bias voltage specified in this test method.

FIG. 1 Relationships Between Depletion Depth, Applied Reverse Bias Voltage, and Dopant Density

Determine the Precision of a Test Method [5]

F 26 Test Methods for Determining the Orientation of a Semiconductive Single Crystal [6]

F 42 Test Methods for Conductivity Type of Extrinsic Semiconducting Materials [6]

F 81 Test Method for Measuring Radial Resistivity Variation on Silicon Wafers [6]

F 84 Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe [6]

F 419 Test Method for Determining Carrier Density in Silicon Epitaxial Layers by Capacitance-Voltage Measurements on Fabricated Junction or Schottky Diodes [6]

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[6] *Annual Book of ASTM Standards*, Vol 10.05.

F 672 Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe [6]

F 723 Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon [6]

F 1153 Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements [6]

F 1241 Terminology of Silicon Technology [6]

2.2 *SEMI Standards:*

SEMI C28 Specifications for Hydrofluoric Acid [7]

SEMI C29 Specification for Hydrofluoric Acid, 4.9 %[7]

SEMI C30 Specification for Hydrogen Peroxide[7]

3. Terminology

3.1 *Definitions:*

3.1.1 For definitions of terms used in silicon wafer technology refer to Terminology F 1241.

3.1.2 Definitions of the statistical terms *repeatability* and *reproducibility* are given in Practice E 691.

3.2 *Definitions of Terms Specific to This Standard:*

3.2.1 *compensation capacitance,* C_{comp}— the sum of the stray capacitance of the measurement system and the peripheral capacitance of the mercury probe contact (see 10.3).

3.2.2 *low-resistance contact*—an electrically and mechanically stable contact **(3)** in which the resistance across the contact does not result in excessive series resistance as determined in 11.4 (see also 6.4).

3.2.2.1 *Discussion*—a low-resistance contact may usually be achieved by using a metal-semiconductor contact with an area much larger than that of the mercury probe contact.

3.2.3 *mercury probe contact*—a Schottky barrier diode formed by bringing a column of mercury into contact with an appropriately prepared polished or epitaxial silicon surface.

4. Summary of Test Method

4.1 The compensation capacitance and effective mercury probe contact area are determined using a reference wafer.

4.2 The test specimen is placed in the mercury probe fixture. A column of mercury is brought into contact with the epitaxial or polished surface of the specimen by a pressure differential between the mercury and ambient to form a Schottky barrier diode (mercury probe contact).

4.3 A low-resistance return contact is also made to either the front or back surface of the wafer. This contact may be either a metal plate or a second mercury-silicon contact with an area much larger than the mercury probe contact.

4.4 The quality of the Schottky barrier diode formed by the mercury probe contact is evaluated by measuring its series resistance and its reverse current characteristics.

4.5 The small-signal, high frequency capacitance of the mercury probe contact is measured as a function of the voltage applied between the mercury probe column and the return contact. The polarity of the applied voltage is such that the mercury probe contact is reverse biased and the low-resistance return contact is forward biased.

4.6 The net carrier density profile (net carrier density as a function of depth from the surface) is calculated from the measured values of capacitance and applied voltage by one of two equivalent methods.

NOTE 3—Net carrier density values obtained by this test method are often converted to resistivity, which is generally a more familiar parameter in the industry. If this is done, the conversion should be made in accordance with the computational methods given in 7.2 of Practice F 723 (conversion from dopant density to resistivity). Note that in applying this conversion procedure in either direction it is assumed that the net carrier density is equal to the dopant density.

5. Significance and Use

5.1 This test method can be used for research and development, process control, and materials specification, evaluation, and acceptance purposes. However, in the absence of interlaboratory test data to establish its reproducibility, this test method should be used for materials specification and acceptance only after the parties to the test have established reproducibility and correlation.

6. Interferences

6.1 A poor Schottky contact, which is generally indicated by an excessively high leakage current (see 11.5) is the most common problem in capacitance-voltage measurements made with mercury probe instruments. It must be emphasized that the use of a poor Schottky contact does not actually prevent a carrier density determination but produces an erroneous result.

6.2 Improper determination of the compensation capacitance, C_{comp}, (see 10.3) can cause significant errors in the capacitance measurement. In homogeneous material, improper zeroing or use of an improper value for C_{comp} results in an apparent monotonic increase or decrease of carrier density with distance from the Schottky barrier. In some fixtures, inherently large stray capacitances exist; in such cases, the value of C_{comp} may depend both on the diameter of the wafer and on the position of the wafer on the chuck. If these dependencies are observed, they may be reduced or eliminated by shielding the mercury probe column. If shielding is not practical, probe calibration procedures should be carried out with wafers of the same diameter as the wafers being tested and care should be taken to ensure that the geometry of wafer and probe is the same during calibration and measurement.

6.3 Alternating frequency test signals greater than 0.05 V rms may lead to errors in the measured capacitance.

6.4 Excessive series resistance in the capacitance measurement circuit can cause significant errors in the measured capacitance values. Series resistance values greater than 1 kΩ have been reported to cause measurement error in some cases **(4, 5)**. The primary source of excessive series resistance is generally a high-resistance return contact; other possible sources are bulk resistance in the wafer and wiring defects in the mercury probe fixture or the test cables (see 11.4).

6.5 When exposed to air, a scum tends to form on the exposed surface of the mercury used to form the mercury probe contact. When freed from the surface, this scum floats to the top of the mercury column. It is necessary to make certain that

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[7] Available from Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043.